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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/673,479	10/16/2000	Nobuaki Hashimoto	107280	6925
25944	7590	01/27/2005	EXAMINER	
OLIFF & BERRIDGE, PLC				GRAYBILL, DAVID E
P.O. BOX 19928				PAPER NUMBER
ALEXANDRIA, VA 22320				2822

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/673,479	HASHIMOTO, NOBUAKI	
	<b>Examiner</b>	<b>Art Unit</b>	
	David E Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 21 December 2004.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 15, 16, 19, 20 and 29-45 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 15, 16, 19, 20 and 29-45 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 16 October 2000 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11-1-4 has been entered.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of claims 29, 33, 34, 39, 40 must be shown or the features canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The

replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 30, 32-35 and 38-42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The claims contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

The undescribed subject matter includes the embodiments comprising the claim 15 limitation of a coefficient of thermal expansion of the first layer being smaller than a coefficient of thermal expansion of the second layer in combination with the limitations of claims 30 and 32-35. The undescribed subject matter also includes the embodiments comprising the claim 36

limitation wherein a modulus of elasticity of the second layer is smaller than a modulus of elasticity of the first layer in combination with the limitations of claims 38-42.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 15, 16, 20, 29-42 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Tsukagoshi (5120665) and Suzuki (6049038).

At column 5, line 56 to column 6, line 41; column 7, lines 8-11; column 8, line 1 to column 9, line 9; column 11, lines 46-49; column 11, line 60 to column 13, line 30; column 14, lines 24-65; column 17, lines 11-21; and column 20, line 51 to column 21, line 33, Tsukagoshi discloses the following:

A semiconductor device comprising: a semiconductor chip 11; a substrate 14 on which a interconnecting pattern 15 is formed; and a binder electrically connecting the semiconductor chip and the interconnecting pattern, the binder including: a first layer 16 including a first resin; and a second layer 18 including conductive particles dispersed only in a second resin, the second layer being disposed closer to the substrate than the first layer; wherein the binder is an anisotropic conductive film; wherein the second layer includes an epoxy resin; wherein conductive particles 3 are dispersed only in the second layer; wherein the conductive particles are dispersed only in the second layer; and wherein the second layer is thinner than the first layer, and the second layer has higher viscosity than the first layer when melted; at least the first resin including an epoxy resin; and electronic equipment 11 comprising the semiconductor device.

A semiconductor device comprising: a semiconductor chip; a substrate on which a interconnecting pattern is formed; and a binder electrically connecting the semiconductor chip and the interconnecting pattern, the binder including: a first layer including a first resin; and a second layer including electroconductive particles dispersed only in a second resin, the second layer being disposed closer to the substrate than the first layer; wherein the binder is an anisotropic conductive film; wherein the second resin includes an epoxy resin; wherein conductive particles are dispersed only in the second layer; and wherein the second layer is thinner than the first layer, and the second layer has higher viscosity than the first layer when melted; and electronic equipment comprising the semiconductor device.

However, Tsukagoshi does not appear to explicitly disclose a coefficient of thermal expansion of the first resin being smaller than a coefficient of thermal expansion of the second resin; wherein a silica insulating filler is mixed only in the first layer; wherein a silica insulating filler is mixed in the first layer and the second layer, and a component ratio of the silica insulating filler in the first layer is greater than a component ratio of the silica insulating filler in the second layer.

Nonetheless, at column 2, lines 14-34; column 3 lines 6-18; column 4, lines 12-61; and column 5, line 57 to column 6, line 24, Suzuki discloses a

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coefficient of thermal expansion of the "first resin" being smaller than a coefficient of thermal expansion of the "second resin"; wherein a silica insulating filler 4 is mixed only in the first layer; wherein a silica insulating filler is mixed in the first layer and the second layer, and a component ratio of the silica insulating filler in the first layer is greater than a component ratio of the silica insulating filler in the second layer. Furthermore, it would have been obvious to combine this product with the product of Tsukagoshi because it would improve the product reliability.

Although Tsukagoshi does not appear to explicitly disclose wherein a modulus of elasticity of the second resin being smaller than a modulus of elasticity of the first resin, the combination of Suzuki and Tsukagoshi discloses a coefficient of thermal expansion of the first resin being smaller than a coefficient of thermal expansion of the second resin, and, as evidenced by Yamada (5959363) at column 3, lines 54-63, filler induced coefficient of thermal expansion and modulus of elasticity of a resin are inherently indirectly correlated.

Claims 19 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukagoshi and Suzuki as applied to claims 15 and 36, and further in combination with Nakamura (6344696).

Tsukagoshi and Suzuki do not appear to explicitly disclose a circuit board on which the semiconductor device is mounted.

Notwithstanding, at column 1, lines 13-36, Nakamura discloses a circuit board "mother board" on which a semiconductor device 2, 14 is mounted. In addition, it would have been obvious to provide the circuit board of Nakamura on which the device of Tsukagoshi and Suzuki is mounted because it would facilitate external electrical connection of the device.

A semiconductor device comprising: a semiconductor chip 11; a substrate 14 on which a interconnecting pattern 15 is formed; and a binder electrically connecting the semiconductor chip and the interconnecting pattern, the binder including: a first layer 16 including a first resin; and a second layer 18 including conductive particles dispersed only in a second resin, the second layer being disposed closer to the substrate than the first layer; wherein the binder is an anisotropic conductive film; wherein the second layer includes an epoxy resin; wherein conductive particles 3 are dispersed only in the second layer; wherein the conductive particles are dispersed only in the second layer; and wherein the second layer is thinner than the first layer, and the second layer has higher viscosity than the first layer when melted; at least the first resin including an epoxy resin; and electronic equipment 11 comprising the semiconductor device.

A semiconductor device comprising: a semiconductor chip; a substrate on which a interconnecting pattern is formed; and a binder electrically

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connecting the semiconductor chip and the interconnecting pattern, the binder including: a first layer including a first resin; and a second layer including electroconductive particles dispersed only in a second resin, the second layer being disposed closer to the substrate than the first layer; wherein the binder is an anisotropic conductive film; wherein the second resin includes an epoxy resin; wherein conductive particles are dispersed only in the second layer; and wherein the second layer is thinner than the first layer, and the second layer has higher viscosity than the first layer when melted; and electronic equipment comprising the semiconductor device.

However, Tsukagoshi does not appear to explicitly disclose a coefficient of thermal expansion of the first resin being smaller than a coefficient of thermal expansion of the second resin; wherein a silica insulating filler is mixed only in the first layer; wherein a silica insulating filler is mixed in the first layer and the second layer, and a component ratio of the silica insulating filler in the first layer is greater than a component ratio of the silica insulating filler in the second layer.

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukagoshi and Suzuki as applied to claim 36 supra, and further in combination with Ito (6333206).

Tsukagoshi and Suzuki does not appear to explicitly disclose the second resin including a biphenyl resin.

Still, as cited, both Tsukagoshi and Suzuki disclose the second resin including an epoxy resin. In addition, at column 35, lines 6-21, Ito discloses a biphenyl epoxy resin. Moreover, it would have been obvious to use the biphenyl epoxy resin of Ito as the epoxy resin of Tsukagoshi and Suzuki because it would provide an epoxy resin having desirable properties.

Applicant's amendment and remarks filed 11-1-4 have been fully considered, are addressed by the rejections supra, and are further addressed infra.

Applicant traverses the 35 U.S.C. 112, first paragraph, rejection of claims 30, 32-35 and 38-42 for failing to comply with the written description requirement, and cites specific portions of the instant specification to support the allegation that the claims were described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

This traversal is respectfully traversed because the citations are not directed to the rejected subject matter, and they do not otherwise overcome the rejection.

The remaining arguments merely assert that particular applied prior art references do not disclose particular limitations. However, the particular references are not relied on for the particular disclosures. To this end, it is respectfully submitted that the rejection is not overcome by pointing out that one reference does not teach a particular limitation when the reference is not relied on for that teaching. *In re Lyons* 150 USPQ 741 (CCPA 1966). Moreover, it is well settled that one cannot show non-obviousness by attacking the references individually where, as here, the rejection is based on combinations of references. *In re Keller*, 208 USPQ 871 (CCPA 1981); *In re Young*, 159 USPQ 725 (CCPA 1968).

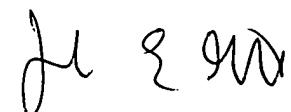
The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

**For information on the status of this application applicant should check PAIR:**

Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.**

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.  
The fax phone number for group 2800 is (703) 872-9306.



David E. Graybill  
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Art Unit 2827

D.G.  
20-Jan-05